FPGA Registers

Standard labZY FPGA Designs

Revision 7.1

Contents

Overview

Applicable Devices

This document applies to the following labZY tools:

nanoMCA

nanoMCA-SP

nanoXRS

nanoDPP

labZY "Tool" refers to any of these devices.

Digital Signals

Digital signals are not continuous. They are defined only at certain instances of time - sampling points. Thus, the digital signals are discrete time signals. Normally the sampling points are equally spaced in time. The time interval between two consecutive sampling points is the sampling period TCLK. The sampling frequency is 1/TCLK.

The values of the digital signal at the sampling points are often referred to as samples. Therefore, the digital signal is a discrete sequence of samples. In practice, each sample is quantified and is represented by a finite number of digital values.

In digital pulse, processing an analog signal from radiation detectors is first digitized (sampled and quantized). The digitization is normally performed by fast ADC operating at sampling frequency from a few tens to a few hundreds of MHz. The sampling frequency of the current labZY tools is 80MHz, corresponding to a sampling period of 12.5ns (TCLK=12.5ns).

The digital signal from the ADC is fed to an FPGA. The FPGA implements all digital pulse processing algorithms. The FPGA designs also include all supporting digital logic, communication functions, and all necessary data storage. The digital pulse processing in the FPGA is performed continuously and in real time. The FPGA pulse processing frequency is the same as the ADC sampling frequency. Therefore, the sampling period TCLK will be used as a unit measure of time when the temporal characteristics of the

digital signals and the associated logic signals have to be related to the continuous time domain.

Fig. 1 shows an example of digital signal. The digital trapezoidal pulse has 3 distinctive temporal features: rise time (RT), flat top (FT), and decay time (DT). For symmetric pulse shapes, DT=RT. Fig. 2 shows the graphical representation of the digital signal of Fig. 1 when the spacing between the samples is very small compared to the total duration of the signal. In this case, the digital signal is represented as a "continuous" line of closely spaced dots. In this document, the digital signals will be drawn as continuous lines only as a graphical presentation of the otherwise quantized, discrete-time domain signals.

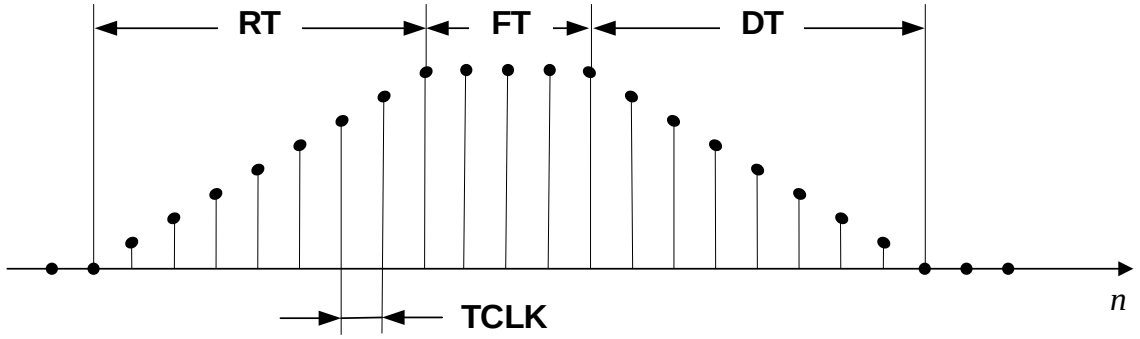


Fig. 1 Digital trapezoidal signal.

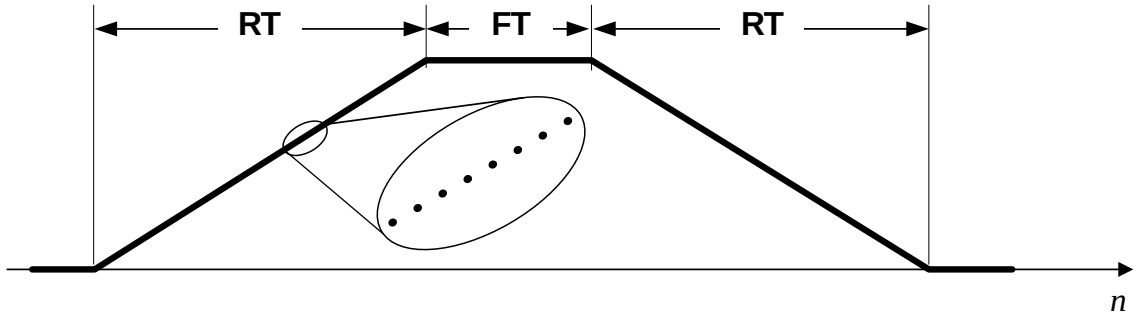


Fig. 2 Graphical representation of the digital trapezoidal signal.

Abbreviations

The following abbreviations are used in the description of the registers accessibility:

RW or **rw** - the registers or the specified bits can be written and read.

RR or **rr** - the registers or the specified bits can only be read. Reading always reports constant preset data. Writing to these registers/bits has no effect on their content but may affect the hardware.

RV or **rv** - the registers or the specified bits can only be read. Reading reports volatile data that is set by the hardware and may change between the readings. Writing to these registers/bits has no effect on their content but may affect the hardware.

WW or **ww** - writing to these registers or the specified bits affects the hardware but is not stored in the register. If the register/bits are read, they always report constant preset data.

WV or **wv** - writing to these registers or the specified bits affects the hardware but is not stored in the register. If the register/bits are read, they report volatile data that is set by the hardware and may change between the readings.

NC or **RESERVED** - the registers or the specified bits can be written and read. They have no effect on the hardware and can be used as scratch pad storage. Note that the NC specification may depend on the FPGA design version. These registers or bits are in general reserved for future expansion of the hardware.

The abbreviations associated with the Register values are alphabetically organized in Apendix A.

Registers

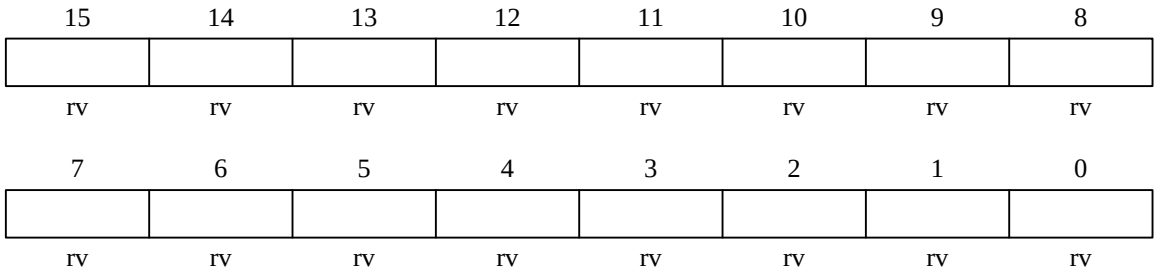
Basics

Physically, the registers are part of the FPGA designs supplied by labZY. Registers are used to control the operation of the labZY Tool with labZY-provided FPGA functionality. The registers are also used to access data such as hardware information, acquisition time, noise measurement, etc. From a software point of view, these registers are 16-bit words. There are 128 registers located at addresses 0x8000 to 0x807F. The address 0x8000 is the base address. Registers are numbered sequentially from 0 to 127. The register number is the offset relative to the base address.

Description

REGISTER 0

Trace Viewer Data (TRVD)

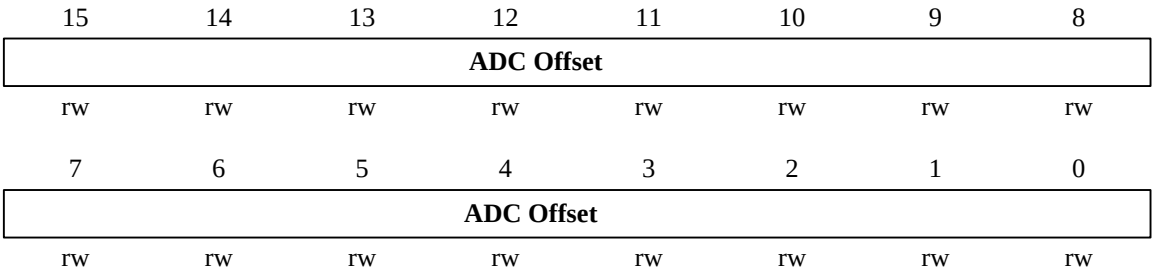


This register is the output of a FIFO register. When this register is read, the address auto-increment bit in the command address field must be set to 0.

The FIFO dept is 512 words (1024 bytes). The even number of words are the signal data (signed), sequentially from left to right (time progression). The odd number of words contain the digital traces data in the lower byte. The upper byte of the odd words should be ignored. Referring to the trace viewer of the labZY-MCA software, Bit 0 of the odd words is the upper (FLLD) trace, bit 7 is the lowest (ROI) trace. Each pair of adjacent even-odd words represent the data at the same clock sample.

REGISTER 1

ADC Offset (ADCO)



ADCO: Bits 15-0**;** Unsigned; Defines the output offset of the ADC.

Refer to the documentation of labZY Tools and labZY-MCA software.

Range: 0 to 32000

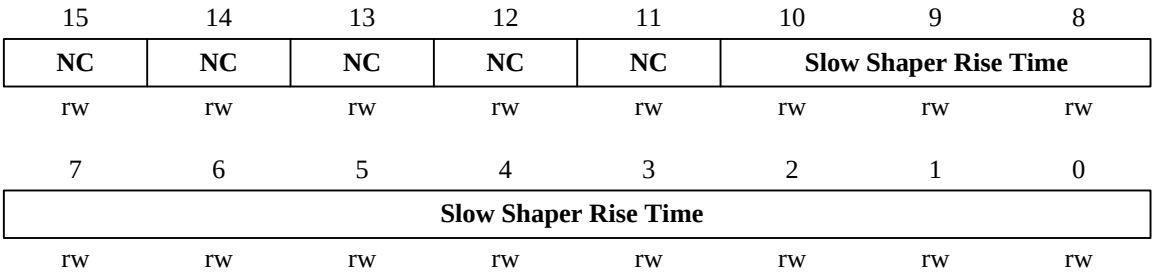
Default: 8000

Dependency: User defined

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.

REGISTER 2

Slow Shaper Rise Time (SSRT)



SSRT: Bits 10-0**;** Unsigned; Defines the number of consecutive samples in the rise time of the slow shaper. The length of the rise time in the time domain is the product of **SSRT** and **TCLK**: **SSRT*TCLK**

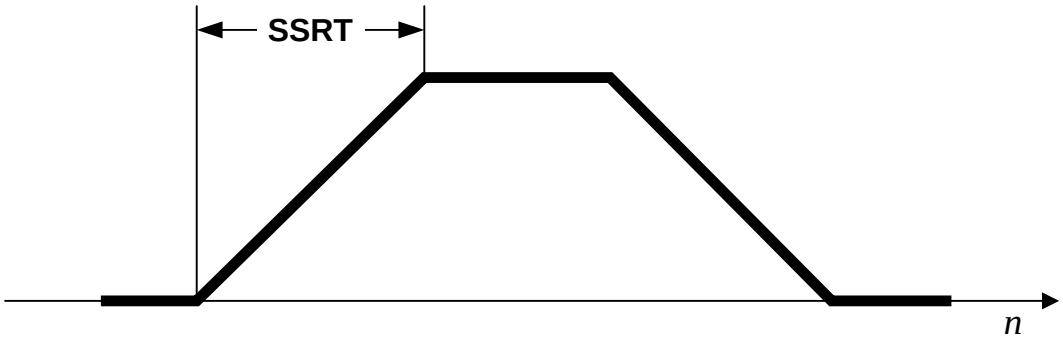
Range: 1 to 2047

Default: 240

Dependency: User defined

Not Connected: Bits 15-11

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.



REGISTER 3

Slow Shaper Flat Top (SSFT)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Slow Shaper Flat Top							
rw	rw	rw	rw	rw	rw	rw	rw

SSFT: Bits 7-0**;** Unsigned; Defines the number of consecutive samples in the flat top of the slow shaper. The length of the flat top in the time domain is the product of **SSFT** and **TCLK**: **SSFT*TCLK**

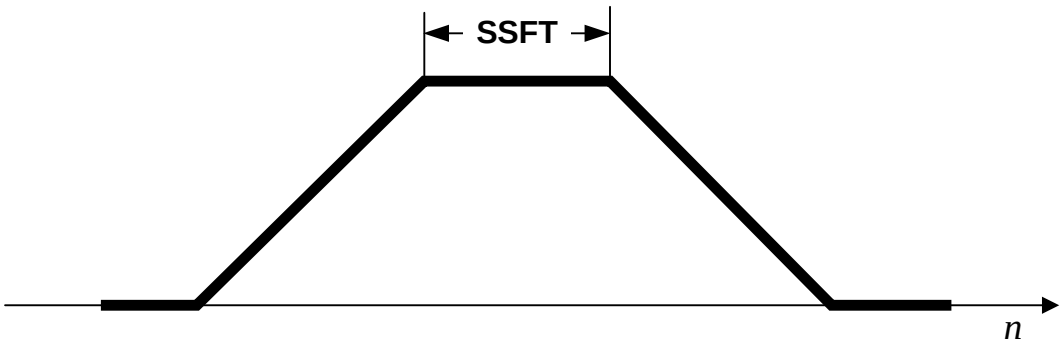
Range: 1 to 255

Default: 1

Dependency: User defined

Not Connected: Bits 15-8

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.



REGISTER 4

Fast Shaper Rise Time (FSRT)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**Fast Shaper Rise Time**	
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Fast Shaper Rise Time							
rw	rw	rw	rw	rw	rw	rw	rw

FSRT: Bits 9-0**;** Unsigned; Defines the number of consecutive samples in the rise time of the fast shaper. The length of the rise time in the time domain is the product of **FSRT** and **TCLK**: **FSRT*TCLK**

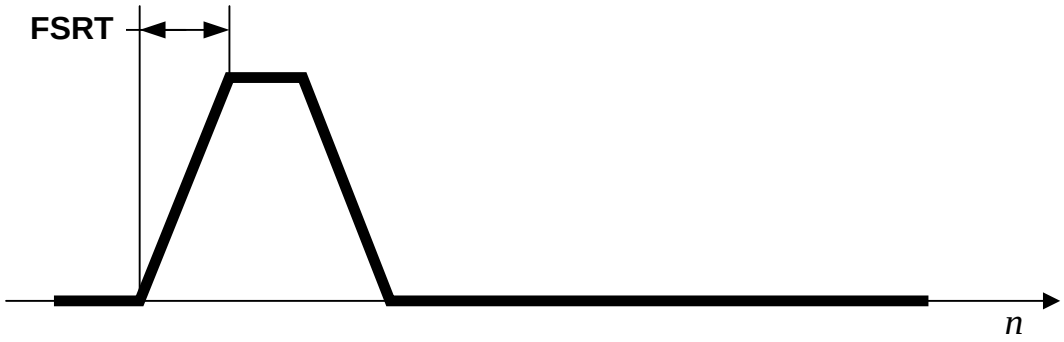
Range: 1 to 1023

Default: 16

Dependency: User defined

Not Connected: Bits 15-10

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.



REGISTER 5

Fast Shaper Flat Top (FSFT)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Fast Shaper Flat Top							
rw	rw	rw	rw	rw	rw	rw	rw

FSFT: Bits 7-0**;** Unsigned; Defines the number of consecutive samples in the flat top of the fast shaper. The length of the flat top in the time domain is the product of **FSFT** and **TCLK**: **FSFT*TCLK**

Range: 1 to 255

Default: 1

Dependency: User defined

Not Connected: Bits 15-8

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.

REGISTER 6

Reserved

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.

REGISTER 7

Reserved

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.

REGISTER 8

Short Time Constant B (STCB)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Short Time Constant B							
rw	rw	rw	rw	rw	rw	rw	rw

STCB: Bits 7-0**;** Unsigned; Defines the secondary unfolding time-constant of the built-in preamplifier (nanoMCA-SP) or the secondary unfolding time-constant of the exponential pulses directly fed to input B (nanoMCA or nanoDPP). The unfolding time constant in the time domain is approximately equal to **STCB*TCLK/8**

Range: 1 to 255

Default: 16

Dependency: User defined

Not Connected: Bits 15-8

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.

REGISTER 9

Long Time Constant B (LTCB)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**Long Time Constant B**				
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Long Time Constant B							
rw	rw	rw	rw	rw	rw	rw	rw

LTCB: Bits 12-0**;** Unsigned; Defines the primary unfolding time-constant of the built-in preamplifier (nanoMCA-SP) or the primary unfolding time-constant of the exponential pulses directly fed to input B (nanoMCA or nanoDPP). The unfolding time constant in the time domain is approximately equal to **LTCB*TCLK/8**

Range: 1 to 8191

Default: 2000

Dependency: User defined

Not Connected: Bits 15-13

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.

REGISTER 10

Short Time Constant A (STCA)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Short Time Constant A							
rw	rw	rw	rw	rw	rw	rw	rw

STCA: Bits 7-0**;** Unsigned; Defines the secondary unfolding time-constant of the built-in amplifier at input A (nanoMCA, nanoMCA-SP, nanoXRS) or the secondary unfolding time-constant of the exponential pulses directly fed to input A (nanoDPP). The unfolding time constant in the time domain is approximately equal to **STCA*TCLK/8**

Range: 1 to 255

Default: 32

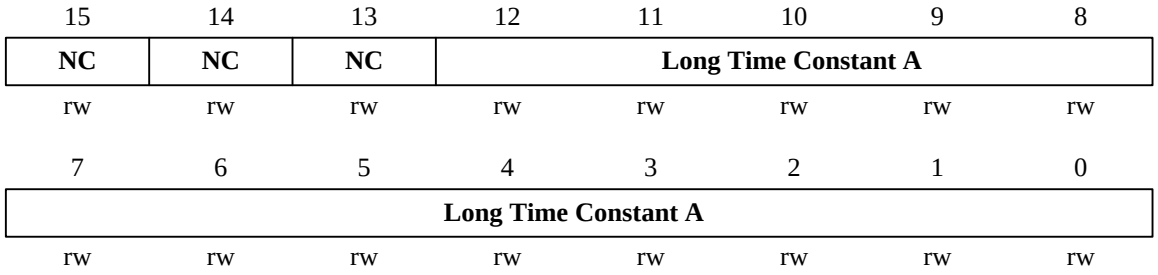
Dependency: User defined

Not Connected: Bits 15-8

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.

REGISTER 11

Long Time Constant A (LTCA)



LTCA: Bits 12-0**;** Unsigned; Defines the primary unfolding time-constant of the built-in amplifier at input A (nanoMCA, nanoMCA-SP, nanoXRS) or the primary unfolding time-constant of the exponential pulses directly fed to input A (nanoDPP). The unfolding time constant in the time domain is approximately equal to **LTCA*TCLK/8**

Range: 1 to 8191

Default: 4000

Dependency: User defined

Not Connected: Bits 15-13

Important: Writing to this register will initialize (reset) the digital pulse processing and the data may be corrupted for up to 100ms. When writing to this register, spectrum acquisition should be disabled for at least 1s or ongoing spectrum acquisition should be restarted with spectral data erased properly.

REGISTER 12

Amplifier Offset (AMPO)

15	14	13	12	11	10	9	8
Amplifier Offset							
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Amplifier Offset							
rw	rw	rw	rw	rw	rw	rw	rw

AMPO: Bits 15-0**;** Unsigned; Defines the offset of the analog signal at the input of the ADC. If the amplifier input is set to positive, then the offset at the ADC input changes proportionally to the **AMPO** value. If the amplifier input is set to negative, then the offset at the ADC input changes inversely to **AMPO** value. It is recommended that **AMPO** is adjusted automatically by setting bit **AOFS** = 1. For given ADC offset **ADCO**, **AMPO** can be adjusted manually so that the baseline of the ADC signal is approximately zero - refer to the www.labzy.com video "Adjusting the Amplifier Offset of nanoMCA tools ".

Range: 0 to 65535

Default: 32768

Dependency: Ignored if bit **AOFS = 1** (Register 16).

REGISTER 13

Fast Discriminator Guard (FDGD)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Fast Discriminator Guard							
rw	rw	rw	rw	rw	rw	rw	rw

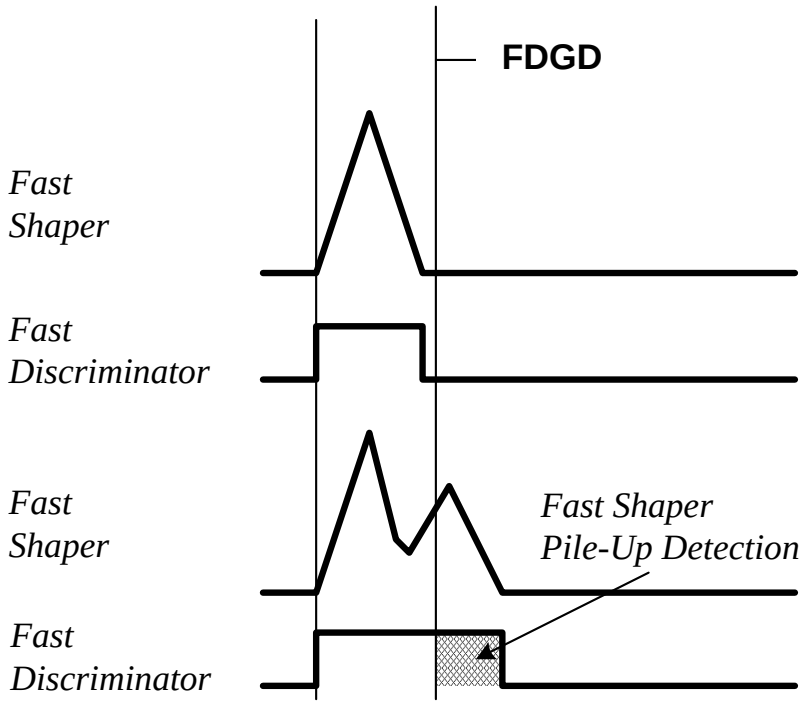
FDGD: Bits 7-0**;** Unsigned; Defines the minimum width of the fast discriminator considered to be pile-up free. When the fast discriminator width is longer than the width specified by this register a pile-up condition in the fast channel is indicated causing a pile-up rejection of the corresponding pulse in the slow channel. This technique effectively reduces the resolving time of the pile-up rejector. However, such pile-up rejection can only be applied when the fast shaper pulses exhibit virtually no tailing. To disable the pile-up rejection based on the fast discriminator width, set **FDGD** = 255 (0xFF). The width of the Fast Discriminator Guard in the time domain is given by **FDGD*TCLK**

Range: 1 to 255

Default: 255

Dependency: User defined

Not Connected: Bits 15-8



REGISTER 14

Input C Inhibit Width (INHW)

15	14	13	12	11	10	9	8
CPOL	**ACPL**	**Input C Inhibit Width**					
rw/rr	rw	rw	rw	rw	rw	rw	rw

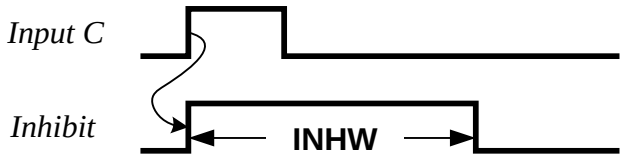
7	6	5	4	3	2	1	0
Input C Inhibit Width							
rw	rw	rw	rw	rw	rw	rw	rw

INHW: Bits 13-0**;** Unsigned; Defines the width of the internal inhibit signal triggered by Input C, **INHW** is in microseconds. If **INHW** is less than the width of the Input C signal, Input C functions as the inhibit signal.

Range: 0 to 10000

Default: 10

Dependency: User defined



ACPL: Bit 14**;** When **ACPL** = 1, the active polarity of the inhibit signal is determined automatically, assuming the average inhibit time is shorter than the non-inhibit time. When **ACPL** = 0 the active polarity of the inhibit signal is determined by the state of the **CPOL** bit.

Default: 1

Dependency: User defined

CPOL: Bit 15**;** When **ACPL** = 0, this bit is ***rw*** and determines the active polarity of the inhibit signal at Input C. When **CPOL** = 0, the active polarity of the inhibit signal at Input C is logic LOW; when **CPOL**=1, the active polarity of the inhibit signal is logic HIGH.

When **ACPL** = 1 this bit is ***rr*** and indicates the automatically determined active polarity of the inhibit signal at Input C. When reading **CPOL** = 0, the active polarity of the inhibit signal at Input C is determined to be logic LOW; when **CPOL** = 1, the active polarity of the inhibit signal is determined to be logic HIGH.

Default: ***rr***

Dependency: User defined or **ACPL** bit.

REGISTER 15

Hardware Info (HINF)

15	14	13	12	11	10	9	8
TOOL				SIZE			
rr	rr	rr	rr	rr	rr	rr	rr

7	6	5	4	3	2	1	0
0	0	0	0	ADFR		ADCR	
rr	rr	rr	rr	rr	rr	rr	rr

ADCR: Bits 1-0**;** Unsigned; ADC resolution in bits:

16 bit ADC - **ADCR**=0;

15 bit ADC - **ADCR**=1;

14 bit ADC - **ADCR**=2;

12 bit ADC - ADCR=3;

ADFR: Bits 3-2**;** Unsigned; ADC sampling frequency (**ADCF**):

ADCF=80MHz - **ADFR**=0;

ADCF=100MHz - **ADFR** =1;

Future Use - **ADFR** =2;

Future Use - **ADFR** =3;

SIZE: Bits 11-8**;** Unsigned; Reports the number of hard size channels (fixed length of the hardware spectrum). The total number of channels is equal to $2^{\mathbf{SIZE}}$

TOOL: Bits 15-22**;** Unsigned; Reports the labZY tool:

nanoXRS - **TOOL**=0;

nanoMCA, nanoMCA-SP - **TOOL**=1;

nanoDPP - **TOOL**=2;

Future Use - **TOOL**= all others

REGISTER 16

Control and Status (CTRS)

15	14	13	12	11	10	9	8
TRVR	DFUN	DPOL	NC	NC	NC	PLSR	AOFS
rv	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
NC	NC	SPCR		LRTM	TMRR	TMRE	ACQE
rw	rw	wv	wv	rw	rw	wv	wv

ACQE: Bit 0**;** Controls Spectrum Acquisition.

Write: Spectrum acquisition is enabled by writing **ACQE** = 1,

Note: Spectrum acquisition will not be enabled if the preset time is reached by the timers.

Spectrum acquisition is disabled by writing **ACQE** = 0.

Read: **ACQE** = 1 when the spectrum acquisition is in progress,

ACQE = 0 when the spectrum acquisition is stopped either manually or by the timers when the preset time is reached.

Default at Power On: Acquisition Disabled

Dependency: User defined or timers.

TMRE: Bit 1**;** Enables/Disables Timers.

Write: Time counting is enabled by writing **TMRE** = 1,

Note: Time counting will not be enabled if the preset time is reached by the timers.

Time counting is disabled by writing **TMRE** = 0.

Read: **TMRE** = 1 when time counting is in progress,

TMRE = 0 when the time counting is stopped, either manually or by the timers when the preset time is reached.

Default at Power On: Time Counting is Disabled

Dependency: User defined or timers.

TMRR: Bit 2**;** Reset Timers.

Write: Reset timers to zero count by writing **TMRR** = 1,

No effect on timers count when writing **TMRR** = 0.

Read: **TMRR**= 0 always.

Dependency: User defined.

LRTM: Bit 3**;** Determines the type of the preset time.

Live Time - **LRTM** = 1,

Real Time - **LRTM** = 0.

Default: 1

Dependency: User defined.

SPCR: Bits 5-4**;** Reset Spectrum Content.

Write: Reset channel counts to zero when writing **SPCR** = 2,

No effect on channel counts when writing any other values.

Read: **SPCR** = 1 always.

Dependency: User defined.

AOFS: Bit 8**;** Amplifier Offset Control.

Automatic - **AOFS** = 1,

Manual - **AOFS** = 0.

Default: 1

Recommended: 1

Dependency: User defined.

PLSR: Bit 9**;** Digital Pulser Control.

Disable Digital Pulser - **PLSR** = 1,

Enable Digital Pulser - **PLSR** = 0.

Default: 1

Dependency: User defined.

DPOL: Bit 13**;** Input D active logic level control.

Active logic LOW - **DPOL** = 0,

Active logic HIGH - **DPOL** = 1.

Default: 0

Dependency: User defined.

DFUN: Bit 14**;** Input D function.

Slow ADC analog input - **DFUN** = 1,

Logic signal input - **DFUN** = 0.

Default: 1

Dependency: User defined.

TRVR: Bit 15**;** Trace Viewer Status Bit.

Trace Viewer Data is Not Ready - **TRVR**=0,

Data is Ready for Download - **TRVR**=1.

REGISTER 17

Fine Analog Gain (FAGN)

15	14	13	12	11	10	9	8
Fine Analog Gain							
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Fine Analog Gain							
rw	rw	rw	rw	rw	rw	rw	rw

FAGN: Bits 15-0**;** Unsigned; Defines the fine gain (***Fine Gain***) of the built-in amplifier.

Fine Gain = 1.2 - **FAGN**/327675

Range: 0 to 65535

Default: 65535

Dependency: User defined

REGISTER 18

Coarse Analog Gain (CAGN)

15	14	13	12	11	10	9	8
IPOL	ISEL	AIPL	NC	NC	NC	NC	NC
rw/rv	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
NC	NC	NC	MUL4	MUL3	MUL2	MUL1	MUL0
rw	rw	rw	rw	rw	rw	rw	rw

MUL0 to MUL4:

nanoMCA and nanoMCA-SP:

Coarse Gain = $1.41^{\mathbf{MUL0}}$+$2.00^{\mathbf{MUL1}}$+$1.19^{\mathbf{MUL2}}$+$4.00^{\mathbf{MUL3}}$+$16.00^{\mathbf{MUL4}}$

nanoXRS and nanoDPP:

Coarse Gain = $1.41^{\mathbf{MUL0}}$+$2.00^{\mathbf{MUL1}}$

All tools:

Total Gain = Coarse Gain* Fine Gain

Dependency: User defined

AIPL: Bit 13**;** When **AIPL** = 1, the polarity of the active input signal is determined automatically. When **AIPL** = 0, the polarity of the active input signal is determined by the state of the IPOL bit.

Default: 1

Dependency: User defined

ISEL: Bit 14**;** Analog Input Select.

Input A is active when **ISEL** = 0,

Input B is active when **ISEL** = 1.

Default: 0

Dependency: User defined.

IPOL: Bit 15**;** When **AIPL** = 0, this bit is ***rw*** and determines the signal polarity the active analog input (A or B). When **IPOL** = 0, the polarity of the analog signal is negative; when **IPOL**=1, the polarity of the analog signal is positive.

When **AIPL** = 1, this bit is ***rr*** and indicates the automatically determined active polarity of the analog signal at active analog input (A or B). When reading **IPOL** = 0, the input analog signal is negative; when **IPOL** = 1, the input analog signal is positive .

Default: ***rr***

Dependency: User defined or **AIPL** bit (Register 18).

REGISTER 19

Pole-Zero (PZRO)

15	14	13	12	11	10	9	8
APZO	**NC**	**NC**	**NC**	**Pole-Zero**			
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Pole-Zero							
rw	rw	rw	rw	rw	rw	rw	rw

PZRO: Bits 11-0**;** Unsigned; Defines the attenuation factor of the pole-zero compensating circuit. Larger numbers of **PZRO** compensate for relatively shorter time constants; smaller numbers of **PZRO** compensate for longer time constant. Set **PZRO**=0 for signals from reset type preamplifiers.

Range: 0 to 4095

Default: 0

Applicable: Input A of nanoMCA and nanoMCA-SP only.

Dependency: User defined

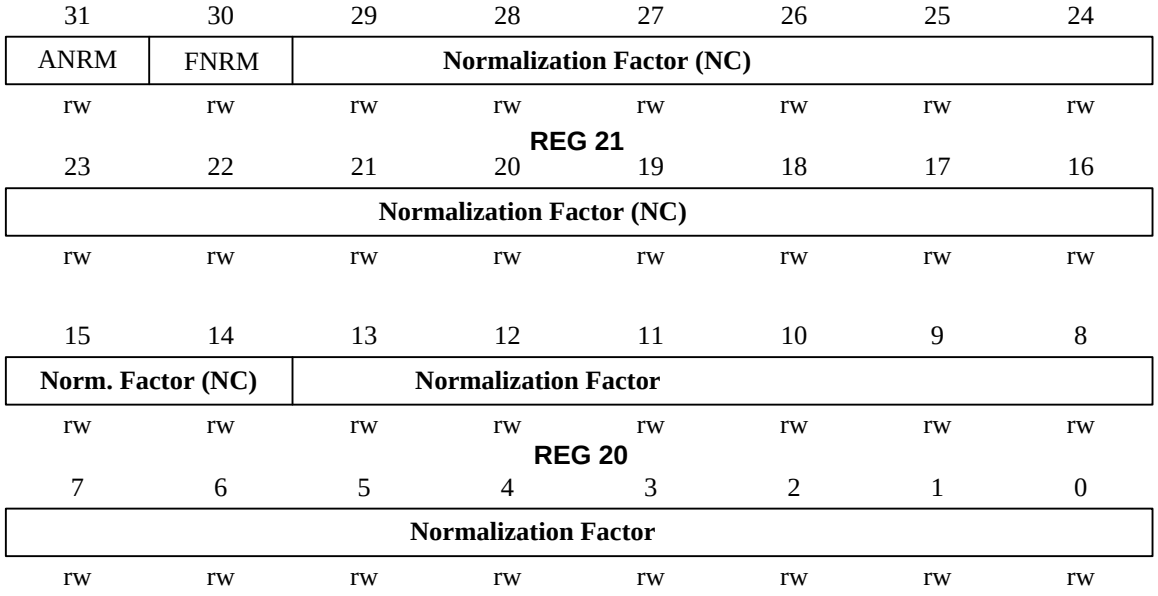
APZO: Bit 15**;** Control for automatic Pole-Zero adjustment. Not implemented at the time of writing this document.

Applicable: nanoMCA and nanoMCA-SP only.

Not Connected: Bits 14-12

REGISTERS 20, 21

Normalization Factor (NORM)



NORM: Bits 13-0**;** Unsigned; Defines the normalization factor used to scale down the pulse-height measurement so that a predefined range of the ADC digitized signal fits within the hard spectrum size.

Range: 0 to 2^{14}-1

Dependency: User defined or automatically calculated depending on the rise time of the digitally shaped pulse. For triangular pulse shape and default ADC offset:

NORM = 40960***SSRT**/$2^{\mathbf{SIZE}}$

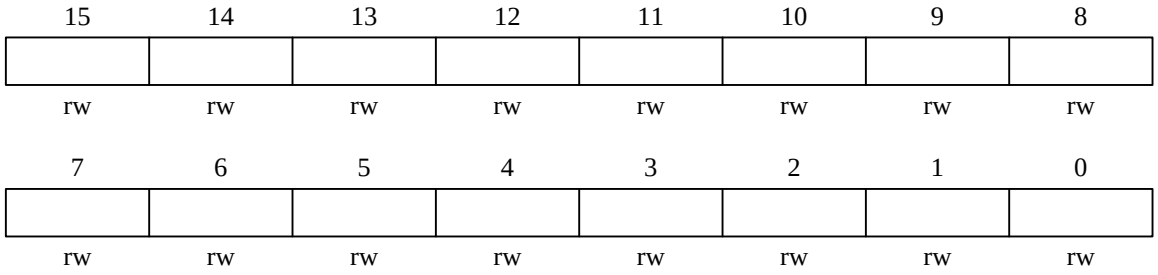
For hard size spectrum of 16k channels **NORM** = 2.5***SSRT** (Register 2).

ANRM: Bit 31**;** This bit has no effect on the hardware. It only indicates to the software to automatically calculate **NORM** as function of **SSRT**.

FNRM: Bit 30**;** This bit has no effect on the hardware. It only indicates to the software to fine calculate **NORM** using time constant dependency.

REGISTER 22

Scratch Pad (DATE)

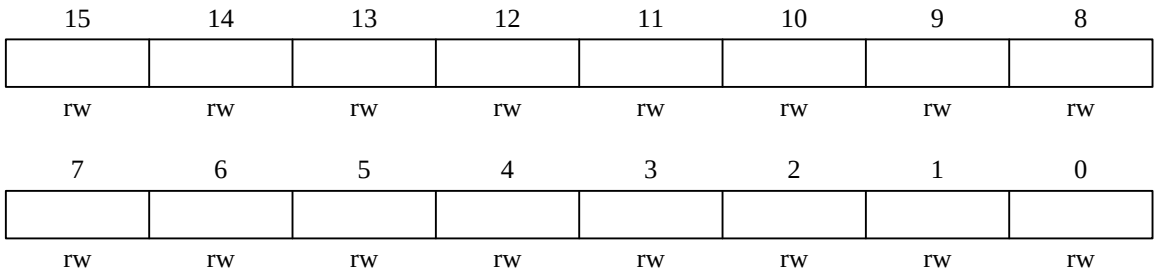


DATE: Bits 15-0**;** This register neither controls nor depends on the hardware. It can be used as a non-volatile storage. The labZY-MCA software stores the Start Date of the spectrum acquisition.

Dependency: User defined

REGISTER 23

Scratch Pad (TIME)



TIME: Bits 15-0**;** This register neither controls nor depends on the hardware. It can be used as a non-volatile storage. The labZY-MCA software stores the Start Time of the spectrum acquisition.

Dependency: User defined

REGISTER 24

Trace Viewer Sampling Frequency Divider (TVFD)

15	14	13	12	11	10	9	8
Trace Viewer Sampling Frequency Divider							
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Trace Viewer Sampling Frequency Divider							
rw	rw	rw	rw	rw	rw	rw	rw

TVFD: Bits 15-0**;** Unsigned; Defines the trace viewer sampling frequency divider. The trace viewer sampling frequency (**TVSF**) is:
TVSF = **ADCF** / (**TVFD** + 1)

Range: 0 to 65535

Default: 0

Dependency: User defined

REGISTER 25

Trace Viewer Pre-Trigger Delay (TVTD)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Trace Viewer Pre-Trigger Delay							
rw	rw	rw	rw	rw	rw	rw	rw

TVTD: Bits 7-0**;** Unsigned; Defines the number of the samples captured by the trace viewer before the active edge of the trace viewer trigger.

Range: 0 to 255

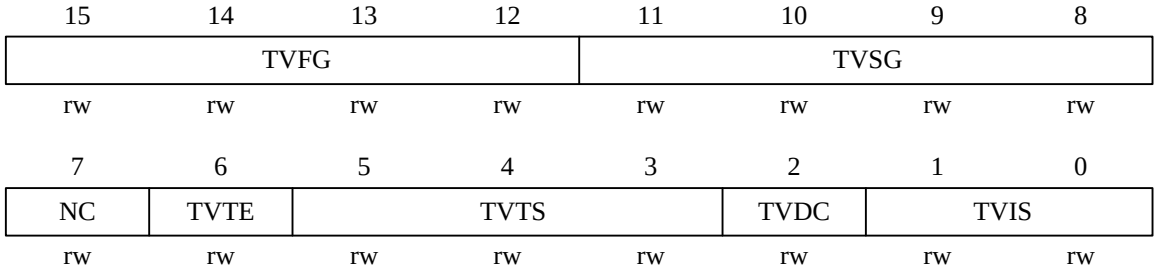
Default: 0

Dependency: User defined

Not Connected: Bits 15-8

REGISTER 26

Trace Viewer Control (TVCT)



TVIS: Bits 1-0**;** Unsigned; Selects the digital signal fed to the input of the trace viewer.

SLOW (shaper) - **TVIS**=0

FAST (shaper) - **TVIS**=1

ADC - **TVIS**=2

AUX (Slow Shaper) - **TVIS**=3

Range: 0 to 3

Default: 0

TVDC: Bit 2**;** Auxiliary trigger source selector. See **TVTS** description.

Default: 0

TVTS: Bits 5-3**;** Unsigned; Selects the trigger source of the trace viewer.

FLLD - **TVTS**=0

SLLD	-	**TVTS**=1
PKDT	-	**TVTS**=2
STORE	-	**TVTS**=3
PUR	-	**TVTS**=4
INHIBIT	-	**TVTS**=5, **TVDC**=0
INPUT C	-	**TVTS**=6, **TVDC**=0
COINC _W	-	**TVTS**=5, **TVDC**=1
INPUT D	-	**TVTS**=6, **TVDC**=1
ROI	-	**TVTS**=7

Default: 0

TVTE: Bit 6**;** Trigger edge selector.

LOW to HIGH	-	**TVTE**=0
HIGH to LOW	-	**TVTE**=1

Default: 0

TVSG: Bits 11-8**;** Unsigned; Gain control of the trace viewer digital signal when the input is fed by the slow shaper (**TVIS**=0).

Trace Viewer Input = (Slow shaper digital signal)/$2^{\mathbf{TVSG}}$

Range: 0 to 15

Default: 0

TVFG: Bits 11-8**;** Unsigned; Gain control of the trace viewer digital signal when the input is fed by the fast shaper (**TVIS**=1).

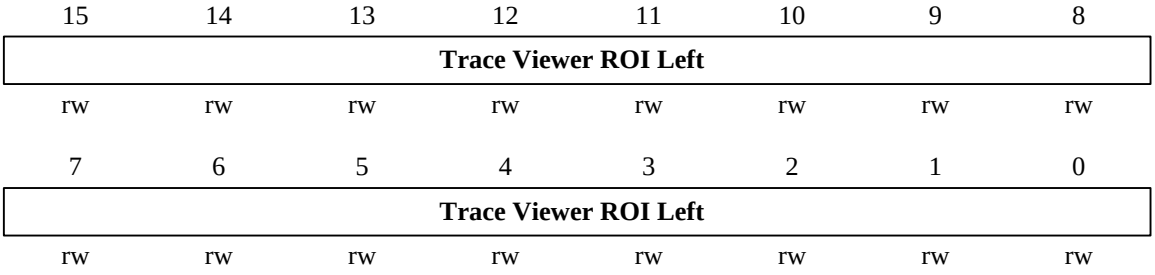
Trace Viewer Input = (Fast shaper digital signal)/$2^{\mathbf{TVFG}}$

Range: 0 to 15

Default: 0

REGISTER 27

Trace Viewer ROI Left (TVRL)



TVRL: Bits 15-0**;** Unsigned; The number of the channel corresponding to the left boundary of an ROI of the hard size spectrum. Pulses whose amplitudes fall within the ROI will trigger the trace viewer when **TVTS**=7.

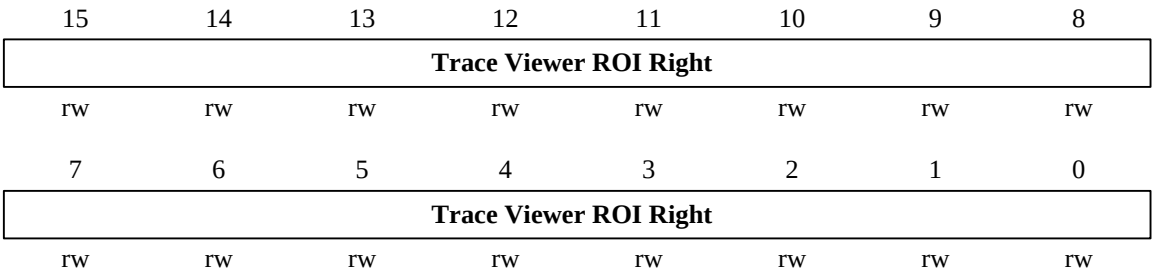
Range: 0 to 16383

Default: 0

Dependency: User defined

REGISTER 28

Trace Viewer ROI Right (TVRR)



TVRR: Bits 15-0**;** Unsigned; The number of the channel corresponding to the right boundary of an ROI of the hard size spectrum. Pulses whose amplitudes fall within the ROI will trigger the trace viewer when **TVTS**=7.

Range: 0 to 16383

Default: 0

Dependency: User defined

REGISTER 29

Reserved

REGISTER 30

Slow Shaper Base-Line Restorer Time Constant (SBLR)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**SBLR**	
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
SBLR							
rw	rw	rw	rw	rw	rw	rw	rw

SBLR: Bits 9-0**;** Unsigned; Defines the time constant of a gated first-order high-pass filter used as a base-line restorer of the slow shaper. The time constant in the time domain is proportional to the product of **SBLR** and **TCLK**: **Time Constant** = **256*SBLR*TCLK**

Range: 1 to 1023

Default: 500

Dependency: User defined

Not Connected: Bits 15-10

REGISTER 31

Fast Shaper Base-Line Restorer Time Constant (FBLR)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
FBLR							
rw	rw	rw	rw	rw	rw	rw	rw

FBLR: Bits 7-0**;** Unsigned; Defines the time constant of a gated first-order high-pass filter used as a base-line restorer of the fast shaper. The time constant in the time domain is proportional to the product of **FBLR** and **TCLK**: **Time Constant** = **256*FBLR*TCLK**

Range: 1 to 255

Default: 100

Dependency: User defined

Not Connected: Bits 15-8

REGISTER 32

Slow Shaper Peaking Time (SPKT)

15	14	13	12	11	10	9	8
Slow Shaper Peaking Time							
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Slow Shaper Peaking Time							
rw	rw	rw	rw	rw	rw	rw	rw

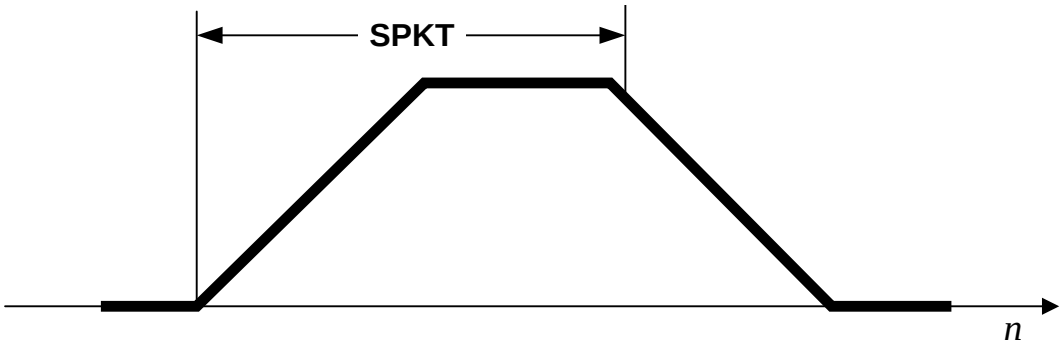
SPKT: Bits 15-0**;** Unsigned; The number of consecutive samples from the beginning of the slow pulse shape to the moment of peak detection. **SPKT** is function of the slow shaper parameters.

SPKT = **SSRT+SSFT+SSRT/32**

Range: Depends on the ranges of **SSRT** and **SSFT**

Default: Calculated from the defaults of **SSRT** and **SSFT**

Dependency: **SSRT** (Register 2) and **SSFT** (Register 3).



REGISTER 33

Slow Shaper Peak Inhibit Time (PINH)

15	14	13	12	11	10	9	8
Slow Shaper Peak Inhibit Time							
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Slow Shaper Peak Inhibit Time							
rw	rw	rw	rw	rw	rw	rw	rw

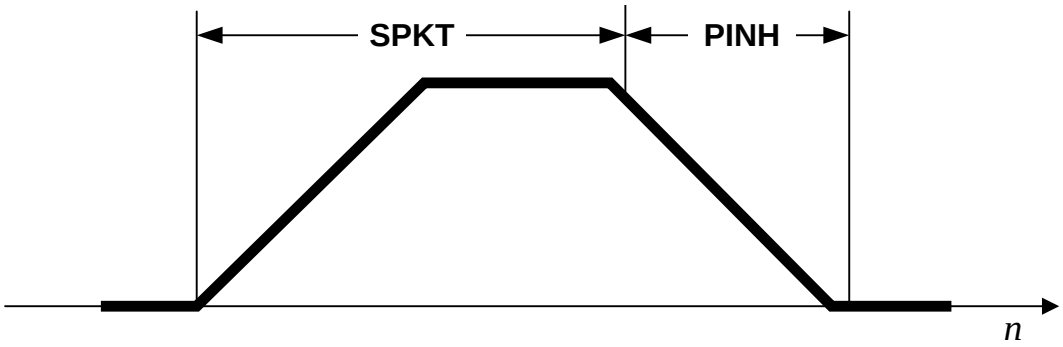
PINH: Bits 15-0**;** Unsigned; The number of consecutive samples from the peak detection until the next allowed peak detection. **PINH** is function of the slow shaper parameters.

PINH = **SSRT- 4,** but not less than zero.

Range: Depends on the range of **SSRT**

Default: Calculated from the default of **SSRT**

Dependency: **SSRT** (Register 2)



REGISTERS 34,35

Slow Shaper Noise Threshold (STHR)

31	30	29	28	27	26	25	24
Slow Threshold							
rw	rw	rw	rw	rw	rw	rw	rw

REG 35

23	22	21	20	19	18	17	16
Slow Threshold							
rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8
Slow Threshold							
rw	rw	rw	rw	rw	rw	rw	rw

REG 34

7	6	5	4	3	2	1	0
Slow Threshold							
rw	rw	rw	rw	rw	rw	rw	rw

STHR: Bits 31-0**;** Signed; The threshold of the slow shaper noise discriminator. **STHR** is set as a function of the desired threshold expressed as a channel number of the hard size spectrum and the normalization factor **NORM**. When set to a negative number, the threshold is set automatically by the hardware.

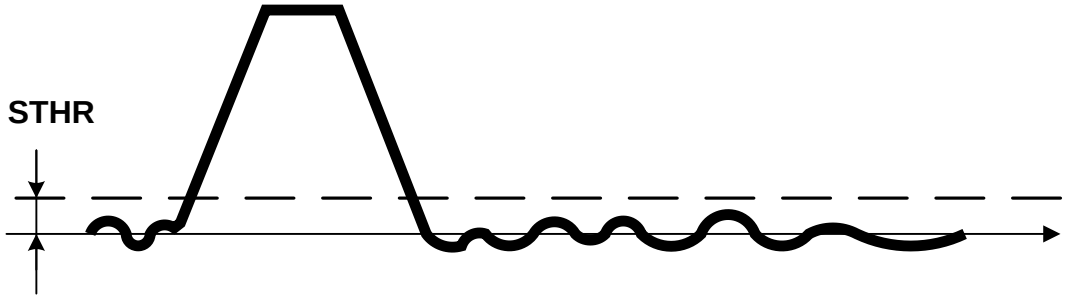
STHR = **(Threshold Channel Number)*NORM** - manual threshold

STHR = -1 - automatic threshold

Range: -1 to 2^{31} -1

Default: -1

Dependency: User defined and **NORM** (Register 20, 21)



REGISTERS 36, 37

Fast Shaper Noise Threshold (FTHR)

31	30	29	28	27	26	25	24
Fast Threshold							
rw	rw	rw	rw	rw	rw	rw	rw

REG 37

23	22	21	20	19	18	17	16
Fast Threshold							
rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8
Fast Threshold							
rw	rw	rw	rw	rw	rw	rw	rw

REG 36

7	6	5	4	3	2	1	0
Fast Threshold							
rw	rw	rw	rw	rw	rw	rw	rw

FTHR: Bits 31-0**;** Signed; The threshold of the fast shaper noise discriminator. **FTHR** is set as a function of the desired threshold

expressed as a channel number of the hard size spectrum and **FSRT** and the **SIZE**. When set to a negative number, the threshold is set automatically by the hardware. Manual setting:

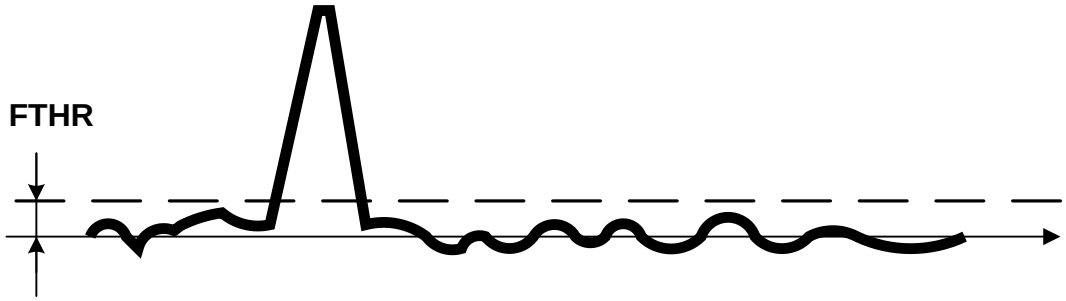
FTHR = **(Threshold Channel Number)*** 40960***FSRT**/2^{SIZE}

FTHR = -1 - automatic threshold

Range: -1 to 2^{31} -1

Default: -1

Dependency: User defined, **FSRT** (Register 4) and **SIZE** (Register 15).



REGISTER 38

Slow Base-Line Restorer Gate (SBGT)

15	14	13	12	11	10	9	8
Slow Base-Line Restorer Gate							
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Slow Base-Line Restorer Gate							
rw	rw	rw	rw	rw	rw	rw	rw

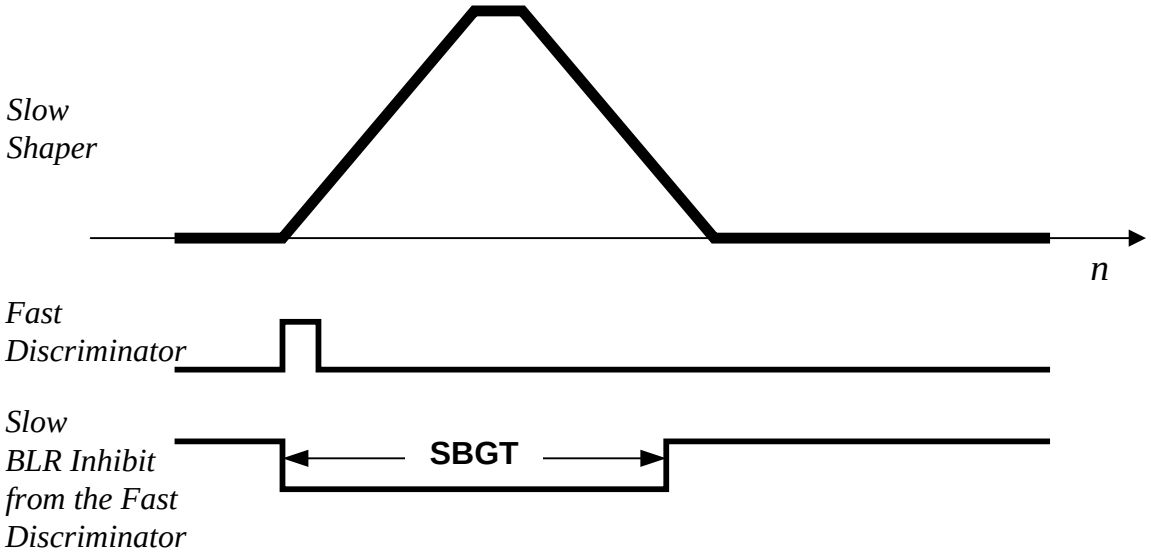
SBGT: Bits 15-0**;** Unsigned; Extension of the fast discriminator signal with number of consecutive samples for which the slow base-line restorer is gated off.

SBGT = **2*SSRT**

Range: Depends on the range of **SSRT**

Default: Calculated from the default of **SSRT**

Dependency: **SSRT** (Register 2)



REGISTER 39

Slow Discriminator Extension (SEXT)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**Slow Discr. Extension**	
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Slow Discriminator Extension							
rw	rw	rw	rw	rw	rw	rw	rw

SEXT: Bits 9-0**;** Unsigned; Extension of the slow shaper noise discriminator signal with specified number of clock periods. The extension length in the time domain is given as:

Extension = **SEXT*TCLK**

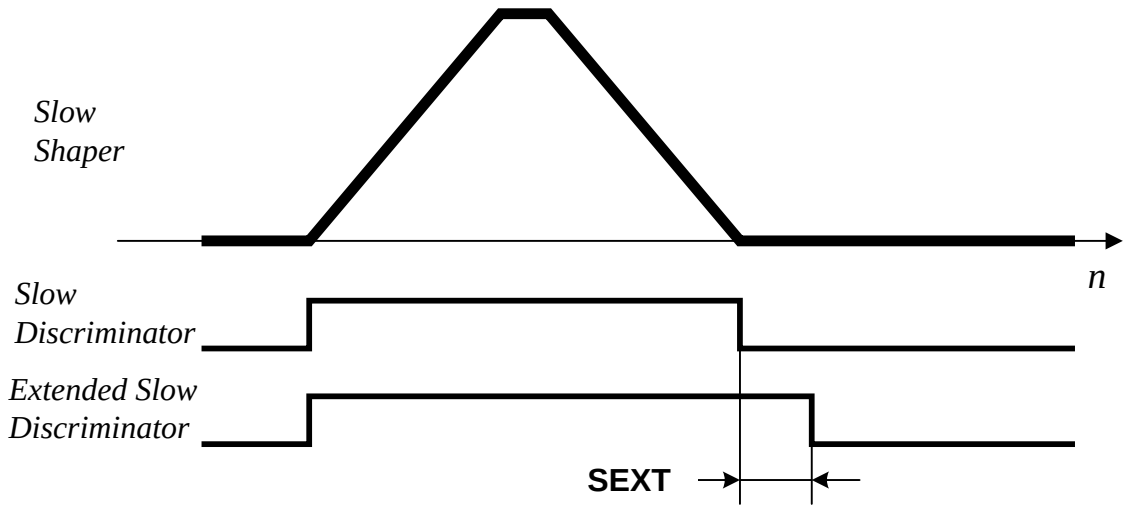
Range: 0 to 1023

Default: **SEXT** = **SSRT/10 + 4**

Recommended: **SEXT** = **SSRT/10 + 4**

Dependency: User defined or **SSRT** (Register 2).

Not Connected: Bits 15-10



REGISTER 40

Fast Discriminator Extension (FEXT)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**	**NC**
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Fast Discriminator Extension							
rw	rw	rw	rw	rw	rw	rw	rw

FEXT: Bits 7-0**;** Unsigned; Extension of the fast shaper noise discriminator signal with specified number of clock periods. The extension length in the time domain is given as:

Extension = **FEXT*TCLK**

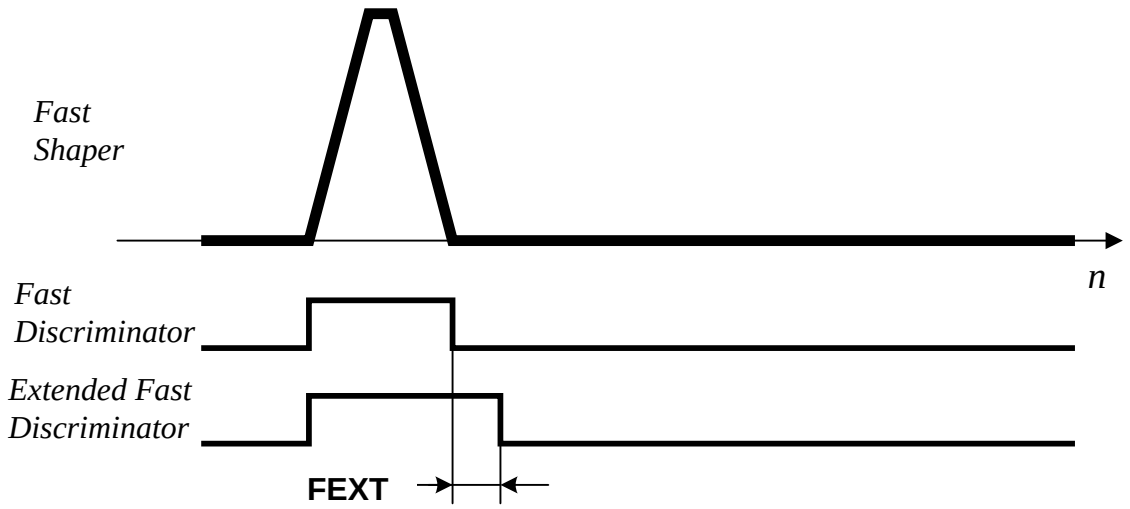
Range: 0 to 255

Default: **FEXT** = **FSRT/10 + 4**

Recommended: **FEXT** = **FSRT/10 + 4**

Dependency: User defined or **FSRT** (Register 4).

Not Connected: Bits 15-8



REGISTER 41

Dead Time Extension (DTEX)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**Dead Time Extension**				
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Dead Time Extension							
rw	rw	rw	rw	rw	rw	rw	rw

DTEX: Bits 12-0**;** Unsigned; Extension of the fast discriminator signal with specified number of clock periods. **DTEX** depends on **FSRT**, **FSFT** and **SPKT**

DTEX = **2* SPKT - (2*FSRT + FSFT)**

Range: 0 to 1023

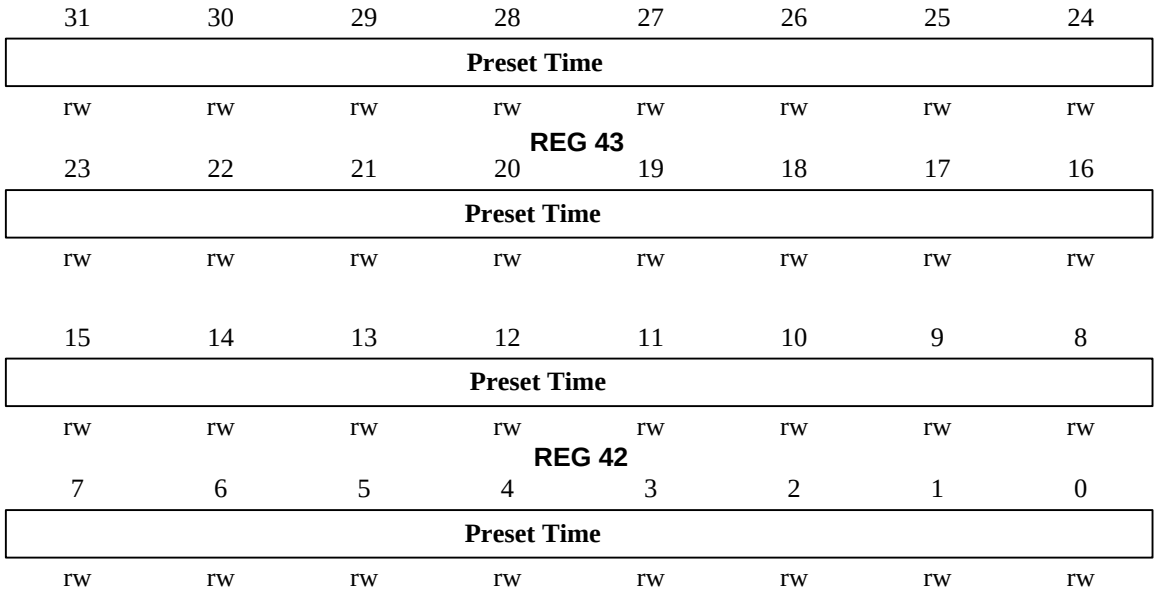
Default: **DTEX** = **2* SPKT - (2*FSRT + FSFT)**

Dependency: **FSRT** (Register 4)**, FSFT** (Register 5)**, SPKT** (Register 32).

Not Connected: Bits 15-13

REGISTERS 42, 43

Preset Time (PRTM)



PRTM: Bits 31-0**;** Unsigned; The preset acquisition time in seconds. Bit **LRTM** determines if the preset time is live time or real time. Set to zero to disable timer control of the spectrum acquisition.

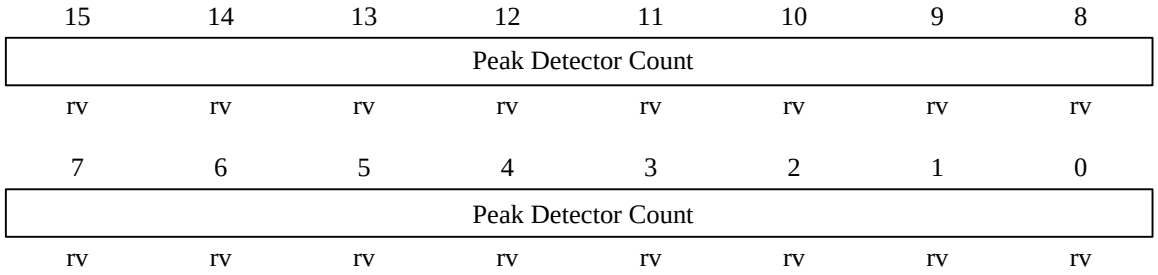
Range: 0 to 2^{32} -1

Default: 0

Dependency: User defined

REGISTER 44

Peak Detector Count (PDCN)



PDCN: Bits 15-0**;** Unsigned; Number of counts peak detected, pile-up free, and stored in the MCA memory in a time interval **ICRR**.

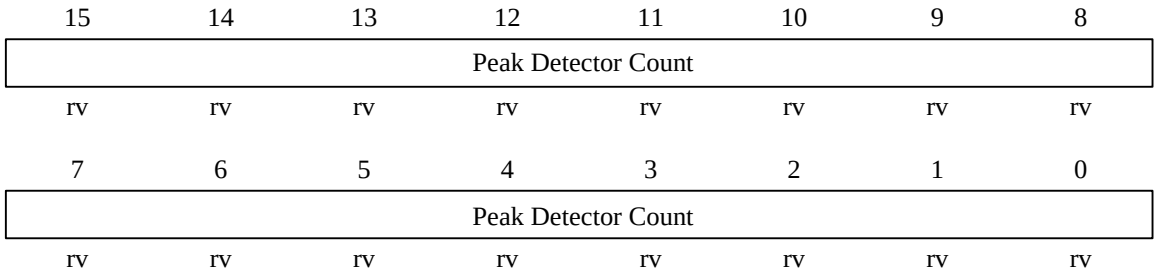
Throughput Count Rate = PDCN/ICRR

Range: 0 to 2^{16} -1

Dependency: Read only

REGISTER 45

Incoming Count (ICRC)



ICRC: Bits 15-0**;** Unsigned; Number of counts of the fast discriminator in a time interval **ICRL**.

True Incoming Count Rate = ICRC/ICRL

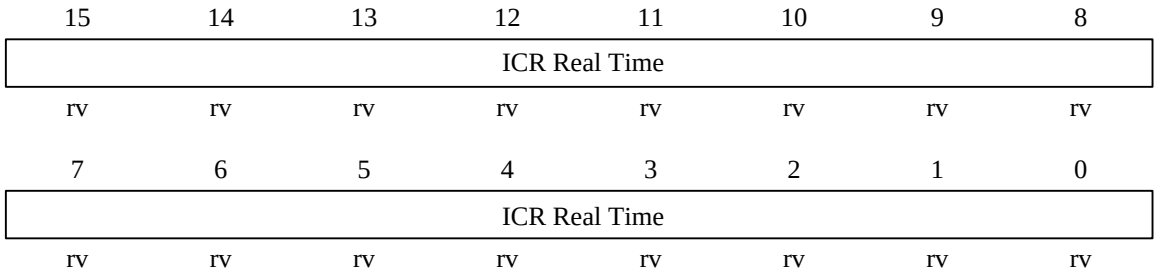
Range: 0 to 2^{16} -1

Dependency: Read only

Unsigned Word representing the number of counts of the fast discriminator in the interval of real time given in REGISTER 46. True incoming rate is calculated by dividing REG 45 by REG 47.

REGISTER 46

ICR Real Time (ICRR)



ICRR: Bits 15-0**;** Unsigned; ICR Real time ticks.

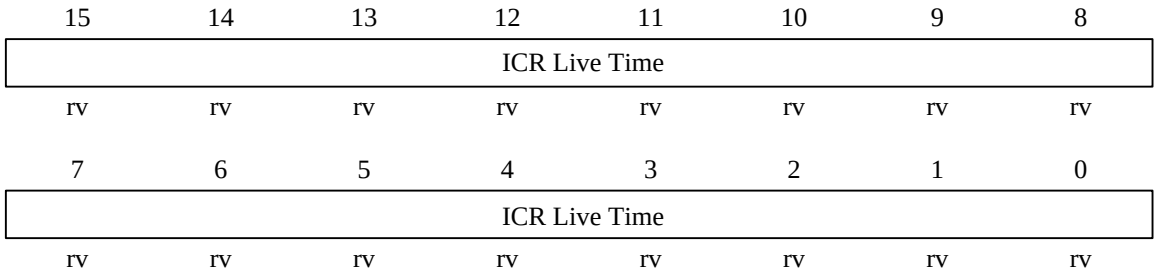
ICR Real Time [seconds] = ICRR * 2048 * TCLK

Range: 0 to 2^{16} -1

Dependency: Read only

REGISTER 47

ICR Live Time (ICRL)



ICRL: Bits 15-0**;** Unsigned; ICR Live time ticks.

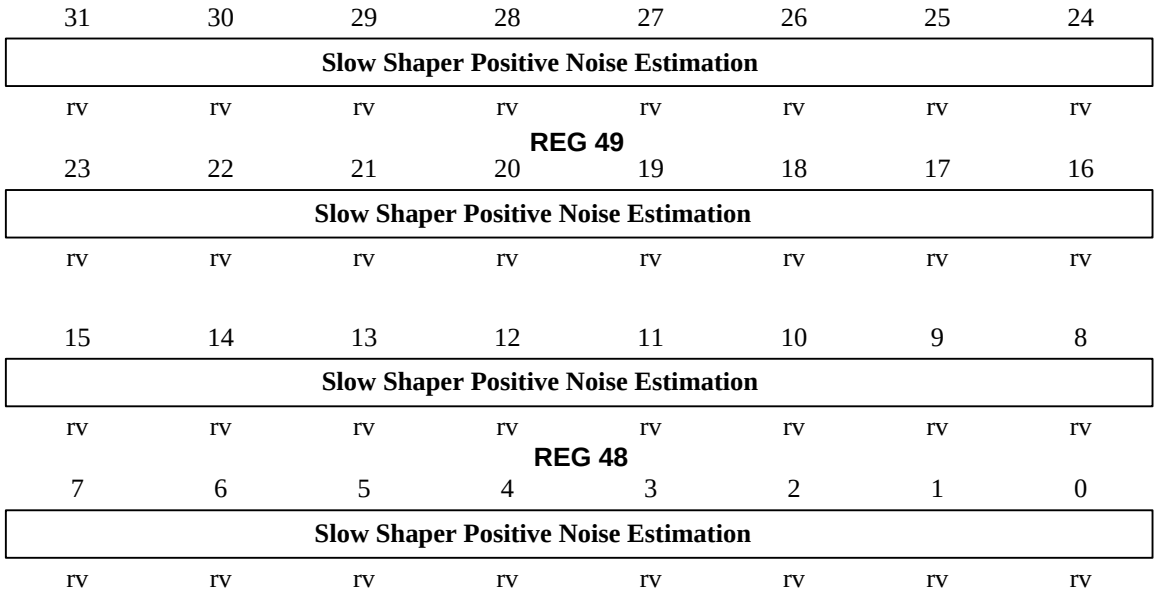
ICR Live Time [seconds] = ICRL * 2048 * TCLK

Range: 0 to 2^{16} -1

Dependency: Read only

REGISTER 48, 49

Slow Shaper Positive Noise Estimation (SPNE)



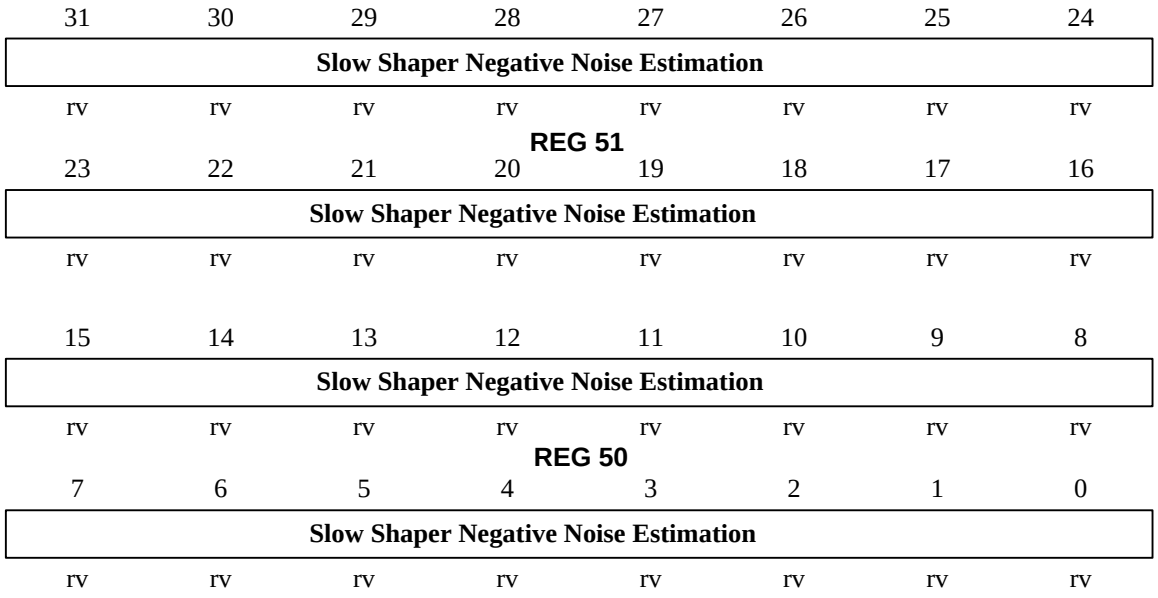
SPNE: Bits 31-0**;** Unsigned; The estimated threshold of the slow shaper noise based on positive noise samples only. The channel number of the hard size spectrum corresponding to the estimated noise threshold can be obtained by dividing the **SPNE** by the normalization factor **NORM**.

Threshold Channel Number = **SPNE/NORM**

Range: 0 to 2^{32} -1

REGISTER 50, 51

Slow Shaper Negative Noise Estimation (SNNE)



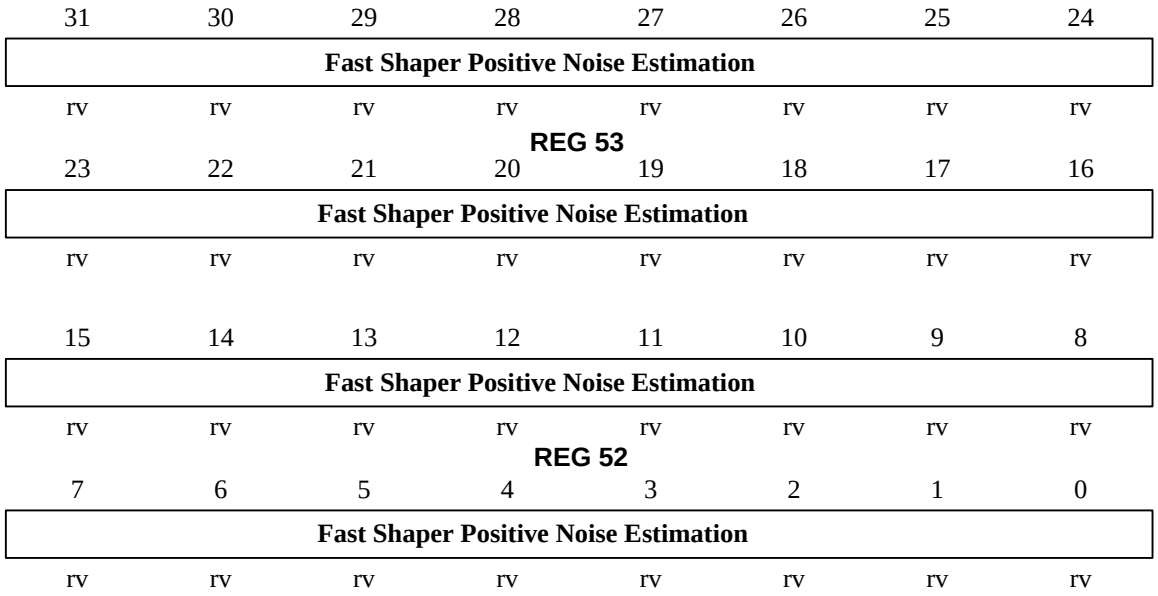
SNNE: Bits 31-0**;** Unsigned; The estimated threshold of the slow shaper noise based on negative noise samples only. The channel number of the hard size spectrum corresponding to the estimated noise threshold can be obtained by dividing the **SNNE** by the normalization factor **NORM**.

Threshold Channel Number = **SNNE/NORM**

Range: 0 to 2^{32} -1

REGISTER 52, 53

Fast Shaper Positive Noise Estimation (FPNE)

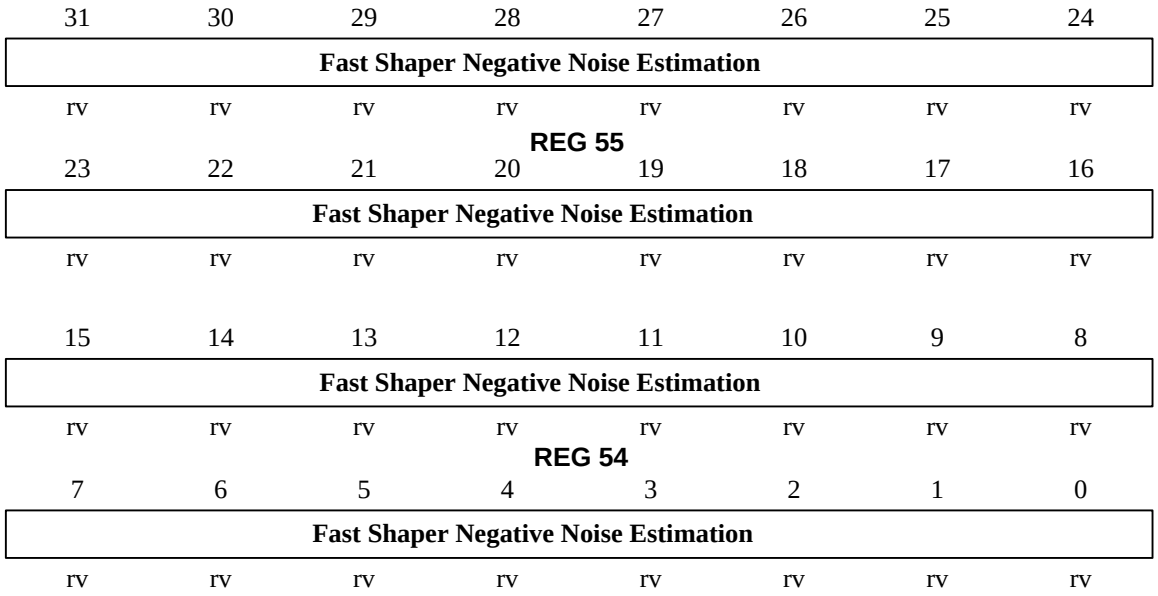


FPNE: Bits 31-0**;** Unsigned; The estimated threshold of the fast shaper noise based on positive noise samples only. The channel number of the hard size spectrum corresponding to the estimated noise threshold can be obtained by dividing the **FPNE** by the normalization factor **NORM**.

Threshold Channel Number = **FPNE/NORM**

Range: 0 to 2^{32} -1

Fast Shaper Negative Noise Estimation (FNNE)

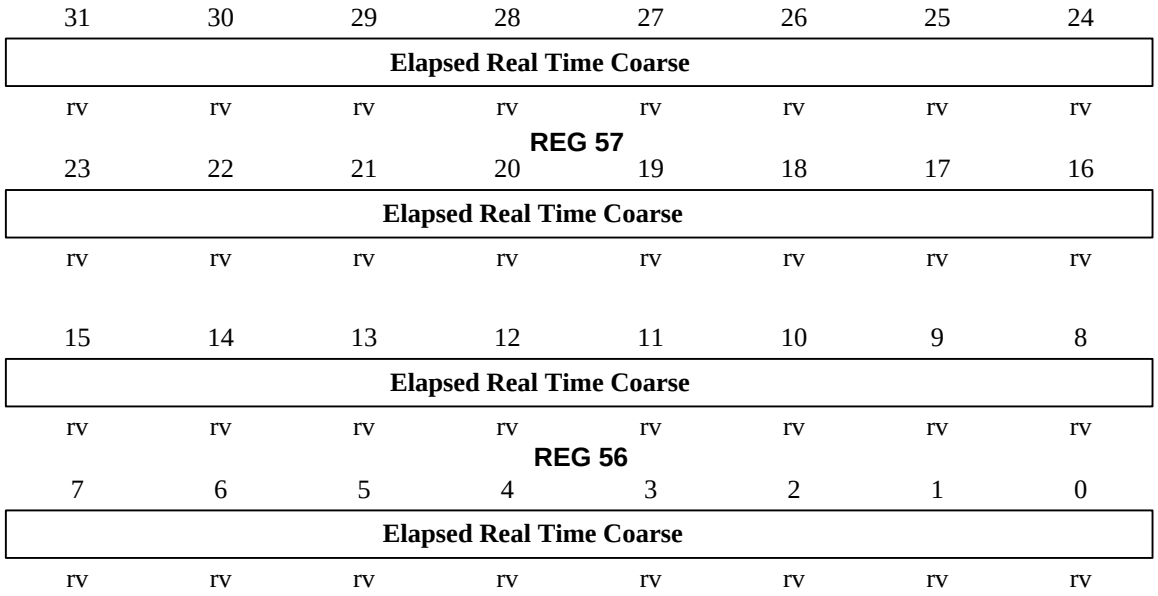


FNNE: Bits 31-0**;** Unsigned; The estimated threshold of the fast shaper noise based on negative noise samples only. The channel number of the hard size spectrum corresponding to the estimated noise threshold can be obtained by dividing the **FNNE** by the normalization factor **NORM**.

Threshold Channel Number = **FNNE/NORM**

Range: 0 to 2^{32} -1

Elapsed Real Time Coarse (ERTC)



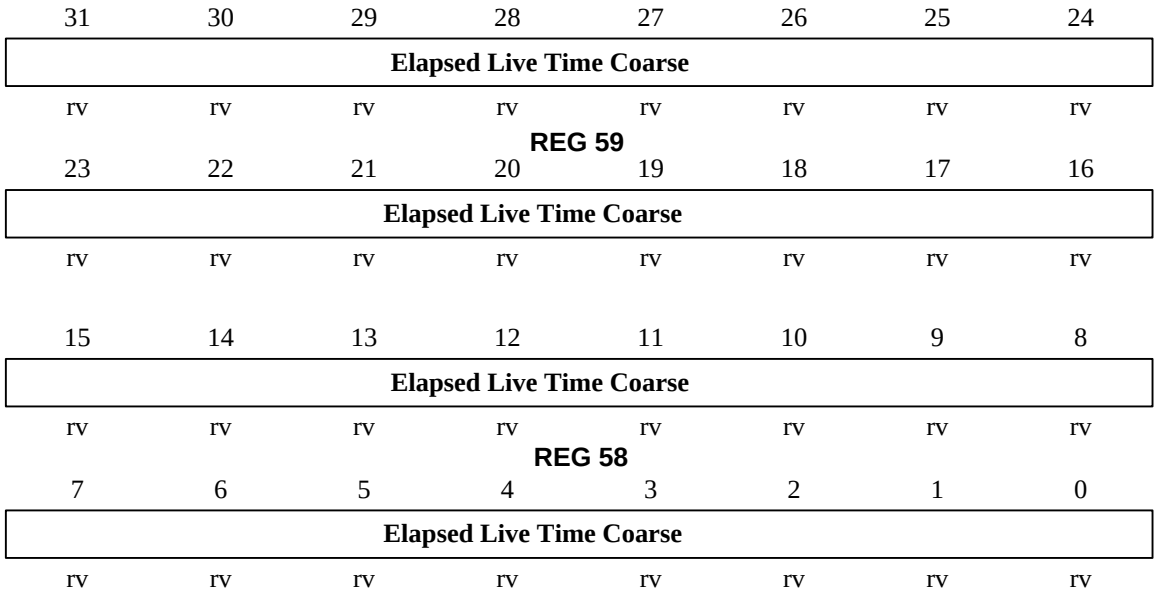
ERTC: Bits 31-0**;** Unsigned; The elapsed real time in increments of 10ms.

The elapsed real time can be calculated with resolution of 200ns using **ERTC** and **ERTF** (Register 60).

Elapsed Real Time [s] = **0.01*ERTC + 0.0000002*ERTF**

Range: 0 to 2^{32} -1

Elapsed Live Time Coarse (ELTC)



ELTC: Bits 31-0**;** Unsigned; The elapsed live time in increments of 10ms.

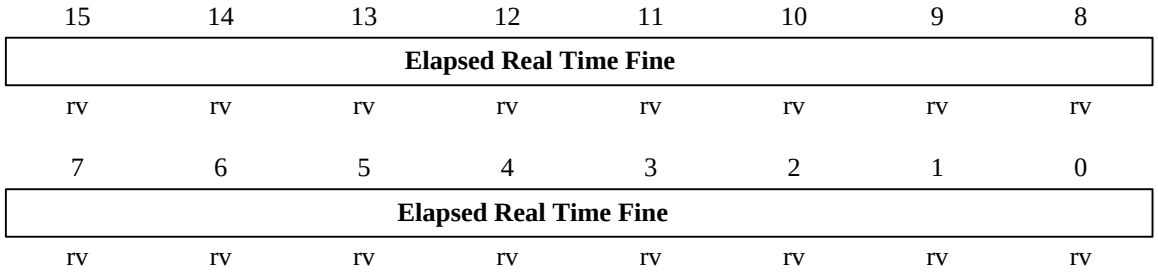
The elapsed live time can be calculated with resolution of 200ns using **ELTC** and **ELTF** (Register 61).

Elapsed Live Time [s] = **0.01*ELTC + 0.0000002*ELTF**

Range: 0 to 2^{32} -1

REGISTER 60

Elapsed Real Time Fine (ERTF)



ERTF: Bits 15-0**;** Unsigned; The elapsed real time in increments of 200ns in the range of 0 to 10ms.

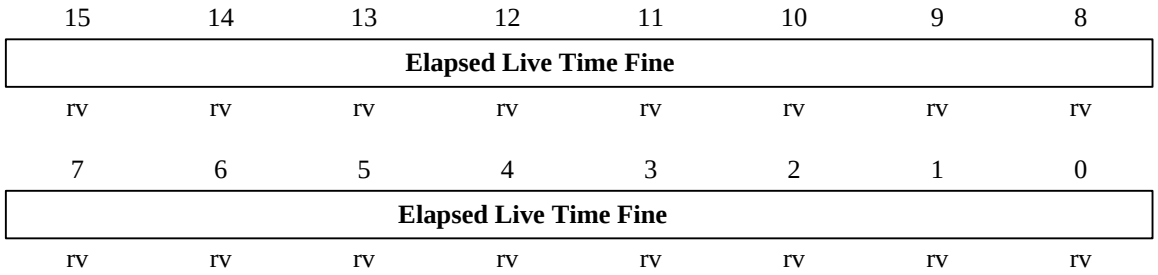
The elapsed real time can be calculated with resolution of 200ns using **ERTF** and **ERTC** (Register 56, 57).

Elapsed Real Time [s] = **0.01*ERTC + 0.0000002*ERTF**

Range: 0 to 49999

REGISTER 61

Elapsed Live Time Fine (ELTF)



ELTF: Bits 15-0**;** Unsigned; The elapsed live time in increments of 200ns in the range of 0 to 10ms.

The elapsed live time can be calculated with resolution of 200ns using **ELTF** and **ELTC** (Register 58, 59).

Elapsed Live Time [s] = **0.01*ELTC + 0.0000002*ELTF**

Range: 0 to 49999

REGISTER 62

Expected Primary Exponential Time Constants

15	14	13	12	11	10	9	8
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
rr	rr	rr	rr	rr	rr	rr	rr

7	6	5	4	3	2	1	0
ETCB				**ETCA**			
rr	rr	rr	rr	rr	rr	rr	rr

ETCA: Bits 3-0**;** Unsigned; Determines the expected Primary Exponential Time Constant at Input A of the labZY tools. This parameter is part of the FPGA design and is specified in the file name of the FPGA design.

Expected Time Constant Input A = 2^{ETCA} ***TCLK**

Range: 0 to 15

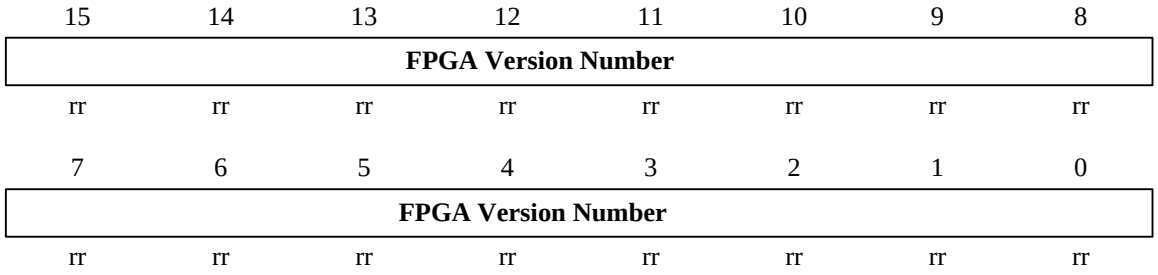
ETCB: Bits 7-4**;** Unsigned; Determines the expected Primary Exponential Time Constant at Input A of the labZY tools. This parameter is part of the FPGA design and is specified in the file name of the FPGA design.

Expected Time Constant Input B = 2^{ETCB} ***TCLK**

Range: 0 to 15

REGISTER 63

FPGA Design Version Number (FPGV)



FPGV: Bits 15-0**;** Unsigned; Specifies the version number of the FPGA design loaded into the labZY tool.

FPGA Version = **FPGV/10.**

Range: 0 to 65535

REGISTER 64

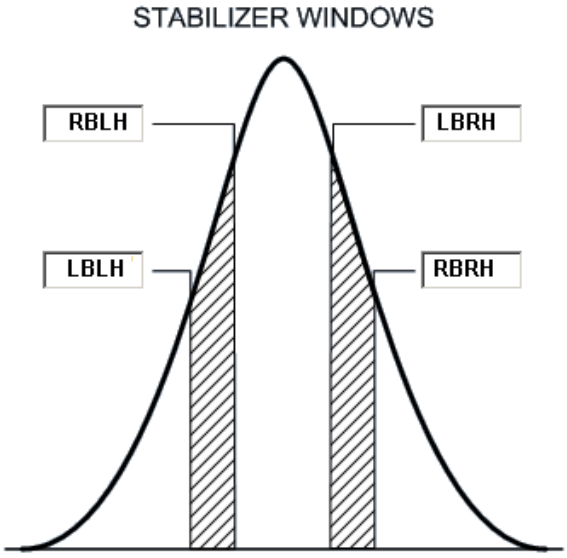
Left Boundary of the Stabilizer Peak Left-Hand Side ROI (LBLH)

15	14	13	12	11	10	9	8
ENST	**NC**	**LBLH**					
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
LBLH							
rw	rw	rw	rw	rw	rw	rw	rw

LBLH: Bits 13-0**;** Unsigned; Channel number of the hard size spectrum corresponding to the left boundary of the stabilizer peak left-hand side ROI.

Range: 0 to 16383

ENST: Bit 15**;** When ENST = 1 the gain stabilizer is enabled. When ENST= 0 the gain stabilizer is disabled.



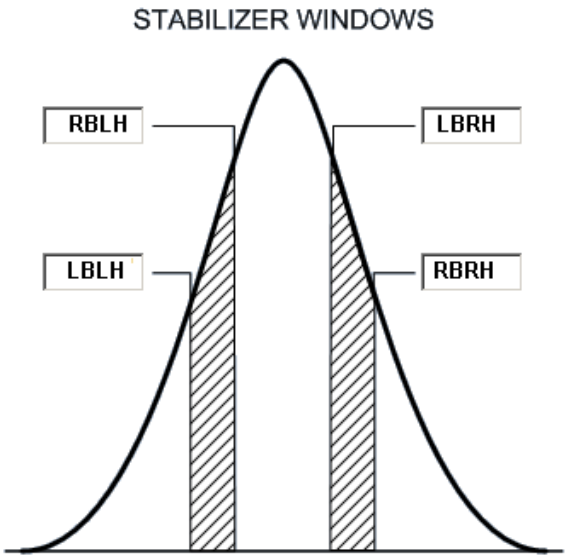
REGISTER 65

Right Boundary of the Stabilizer Peak Left-Hand Side ROI (RBLH)

15	14	13	12	11	10	9	8
NC	**NC**	**RBLH**					
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
RBLH							
rw	rw	rw	rw	rw	rw	rw	rw

RBLH: Bits 13-0**;** Unsigned; Channel number of the hard size spectrum corresponding to the right boundary of the stabilizer peak left-hand side ROI.

Range: 0 to 16383



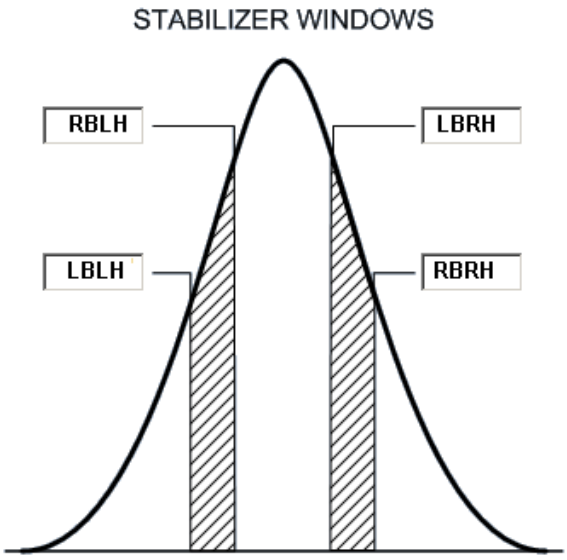
REGISTER 66

Left Boundary of the Stabilizer Peak Right-Hand Side ROI (LBRH)

15	14	13	12	11	10	9	8
NC	**NC**	**LBRH**					
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
LBRH							
rw	rw	rw	rw	rw	rw	rw	rw

LBRH: Bits 13-0**;** Unsigned; Channel number of the hard size spectrum corresponding to the left boundary of the stabilizer peak right-hand side ROI.

Range: 0 to 16383



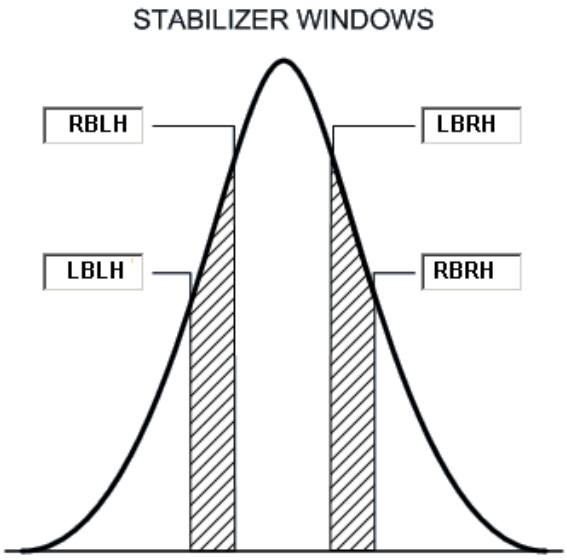
REGISTER 67

Right Boundary of the Stabilizer Peak Right-Hand Side ROI (RBRH)

15	14	13	12	11	10	9	8
NC	**NC**	**RBRH**					
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
RBRH							
rw	rw	rw	rw	rw	rw	rw	rw

RBRH: Bits 13-0**;** Unsigned; Channel number of the hard size spectrum corresponding to the right boundary of the stabilizer peak right-hand side ROI.

Range: 0 to 16383



REGISTER 68

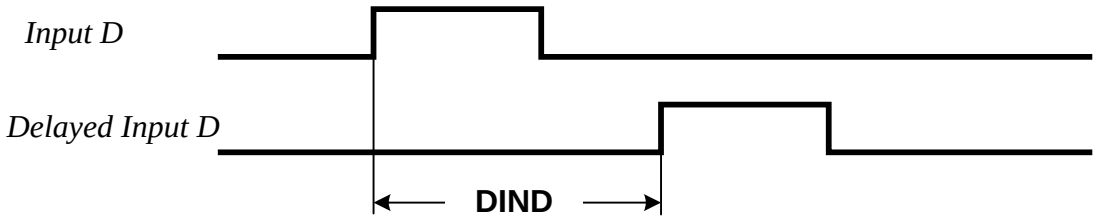
Delay of the Logic Signal at Input D (DIND)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**Delay of the Logic Signal at Input D**			
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Delay of the Logic Signal at Input D							
rw	rw	rw	rw	rw	rw	rw	rw

DIND: Bits 11-0**;** Unsigned; Specifies the delay of the logic signal at the Input D when Input D is configured as logic signal input used for coincidence/anti-coincidence. Not applicable for nanoXRS. In the time domain, the width of the coincidence/anti-coincidence window is:

Input D Delay = **DIND**$_*$**TCLK**

Range: 0 to 4095



REGISTER 69

Coincidence/Anti-Coincidence Window Width (COWW)

15	14	13	12	11	10	9	8
DIRD	**ANTI**	**NC**	**NC**	**Coincidence Window Width**			
rw	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Coincidence Window Width							
rw	rw	rw	rw	rw	rw	rw	rw

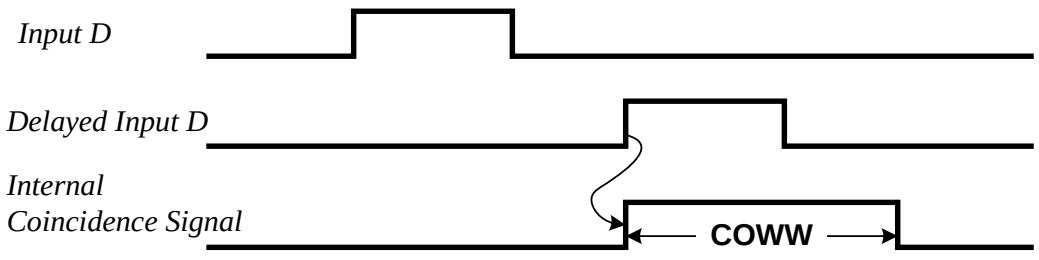
COWW: Bits 11-0**;** Unsigned; Specifies the width coincidence/anti-coincidence window. Not applicable for nanoXRS. In the time domain, the width of the coincidence/anti-coincidence window is:

Window Width = **COWW**$*$**TCLK**

Range: 0 to 4095

DIRD: Bit 15**;** When **DIRD** = 1, the internal window generator is enabled with window width specified by **COWW**. When **DIRD** = 0, the gain window generator is disabled and the width of the Input D logic signal is the width of the coincidence window. Not applicable for nanoXRS.

ANTI: Bit 14**;** When ANTI = 0, the internally generated window is a coincidence window. When ANTI = 1, the internally generated window is an anti-coincidence window. If **DIRD** = 0 then ANTI must also be set to 0. Not applicable for nanoXRS.



REGISTER 70

Pulse-Height Storage Delay (STOD)

15	14	13	12	11	10	9	8
NC	**NC**	**NC**	**NC**	**Pulse-Height Storage Delay**			
rw	rw	rw	rw	rw	rw	rw	rw

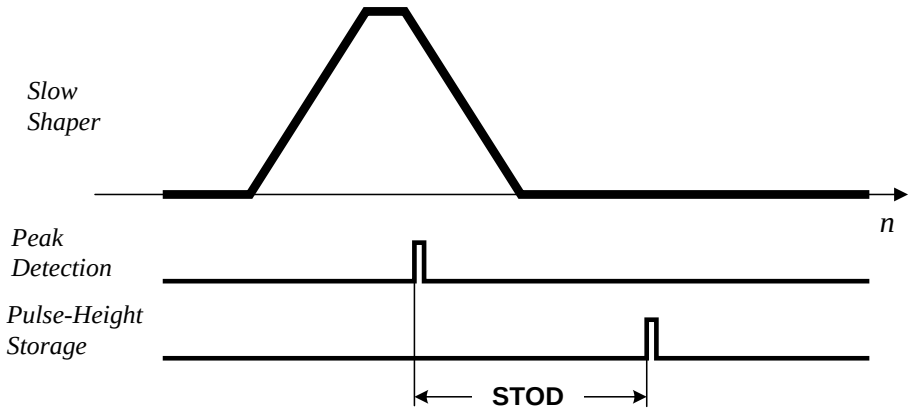
7	6	5	4	3	2	1	0
Pulse-Height Storage Delay							
rw	rw	rw	rw	rw	rw	rw	rw

STOD: Bits 11-0**;** Unsigned; Specifies the delay of pulse height storage and the peak-detect signal. The delayed peak-detect signal is used as coincidence/anti-coincidence signal. Not applicable for nanoXRS.

In the time domain the width of the storage delay is:

Storage Delay = **STOD*TCLK**

Range: 0 to 4095



REGISTER 71 to 127

Reserved

Appendix A: Abbreviations List

ACPL	REGISTER 14
ACQE	REGISTER 16
ADCO	REGISTER 1
ADCR	REGISTER 15
ADFR	REGISTER 15
AIPL	REGISTER 18
AMPO	REGISTER 12
ANRM	REGISTER 20, 21
ANTI	REGISTER 69
AOFS	REGISTER 16
APZO	REGISTER 19
CAGN	REGISTER 18
COWW	REGISTER 69
CPOL	REGISTER 14
CTRS	REGISTER 16
DATE	REGISTER 22
DFUN	REGISTER 16
DIND	REGISTER 68
DIRD	REGISTER 69
DPOL	REGISTER 16
DTEX	REGISTER 41
ELTC	REGISTER 58, 59
ELTF	REGISTER 61
ENST	REGISTER 64
ERTC	REGISTER 56, 57
ERTF	REGISTER 60
ETCA	REGISTER 62
ETCB	REGISTER 62
FAGN	REGISTER 17
FBLR	REGISTER 31

FDGD	REGISTER 13
FEXT	REGISTER 40
FNNE	REGISTER 54, 55
FNRM	REGISTER 20, 21
FPGV	REGISTER 63
FPNE	REGISTER 52, 53
FSFT	REGISTER 5
FSRT	REGISTER 4
FTHR	REGISTER 36, 37
HINF	REGISTER 15
ICRC	REGISTER 45
ICRL	REGISTER 47
ICRR	REGISTER 46
INHW	REGISTER 14
IPOL	REGISTER 18
ISEL	REGISTER 18
LBLH	REGISTER 64
LBRH	REGISTER 66
LRTM	REGISTER 16
LTCA	REGISTER 11
LTCB	REGISTER 9
MUL0 to MUL4	REGISTER 18
NORM	REGISTER 20, 21
PDCN	REGISTER 44
PINH	REGISTER 33
PLSR	REGISTER 16
PRTM	REGISTER 42, 43
PZRO	REGISTER 19
RBLH	REGISTER 65
RBRH	REGISTER 67
SBGT	REGISTER 38
SBLR	REGISTER 30
SEXT	REGISTER 39

SIZE	REGISTER 15
SNNE	REGISTER 50, 51
SPCR	REGISTER 16
SPKT	REGISTER 32
SPNE	REGISTER 48, 49
SSFT	REGISTER 3
SSRT	REGISTER 2
STCA	REGISTER 10
STCB	REGISTER 8
STHR	REGISTER 34, 35
STOD	REGISTER 70
TIME	REGISTER 23
TMRE	REGISTER 16
TMRR	REGISTER 16
TOOL	REGISTER 15
TRVD	REGISTER 0
TRVR	REGISTER 16
TVCT	REGISTER 26
TVDC	REGISTER 26
TVFD	REGISTER 24
TVFG	REGISTER 26
TVIS	REGISTER 26
TVRL	REGISTER 27
TVRR	REGISTER 28
TVSG	REGISTER 26
TVTD	REGISTER 25
TVTE	REGISTER 26
TVTS	REGISTER 26

Revision History

Tracking of the revision history begins with *Revision A1*

Revision A2

Replaced *rr* with *rv* in the register block diagrams fro REGISTERS: 0 and 44 to 61.